Hardware Scheduler Memory Arrangement

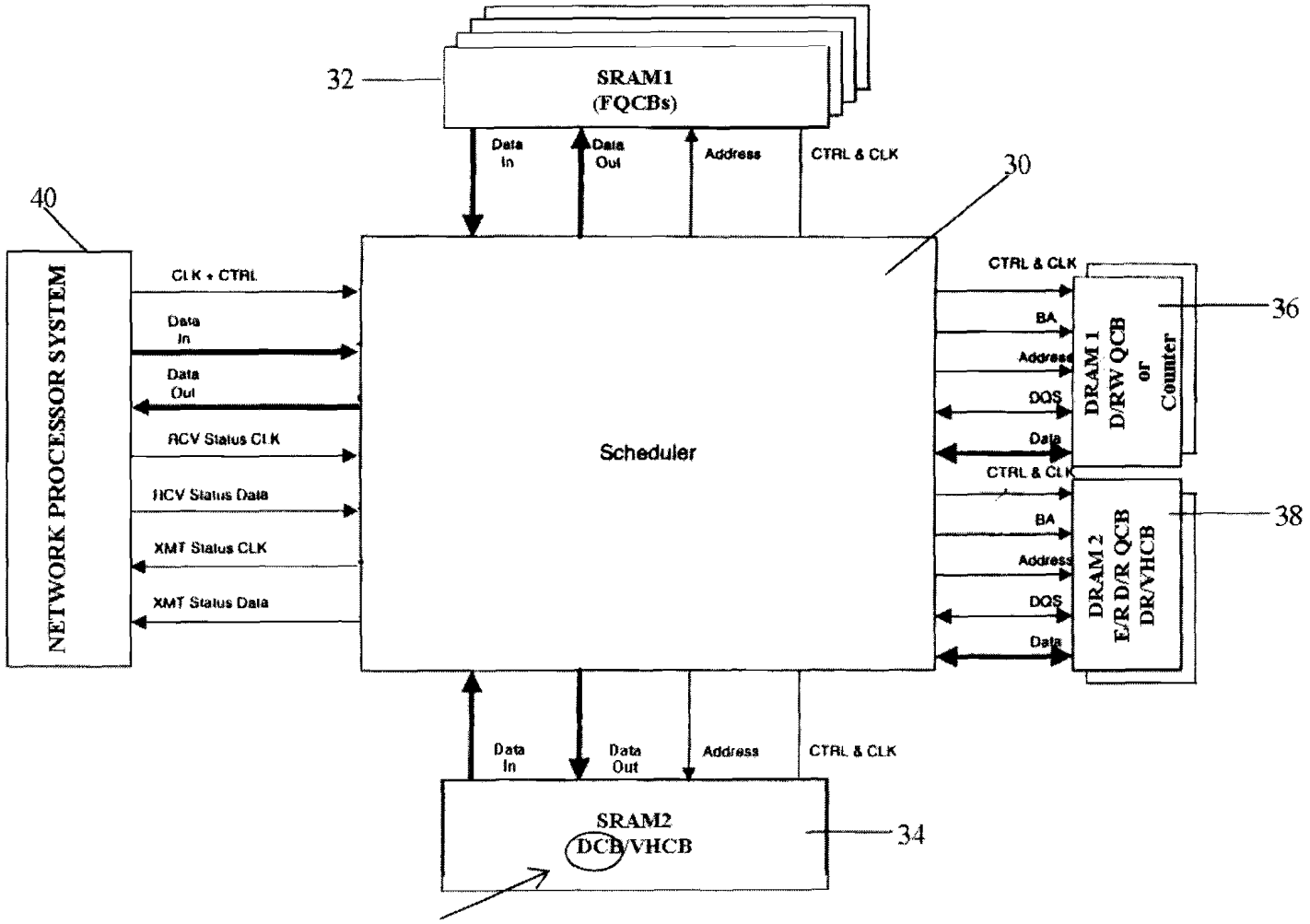

Figure 1

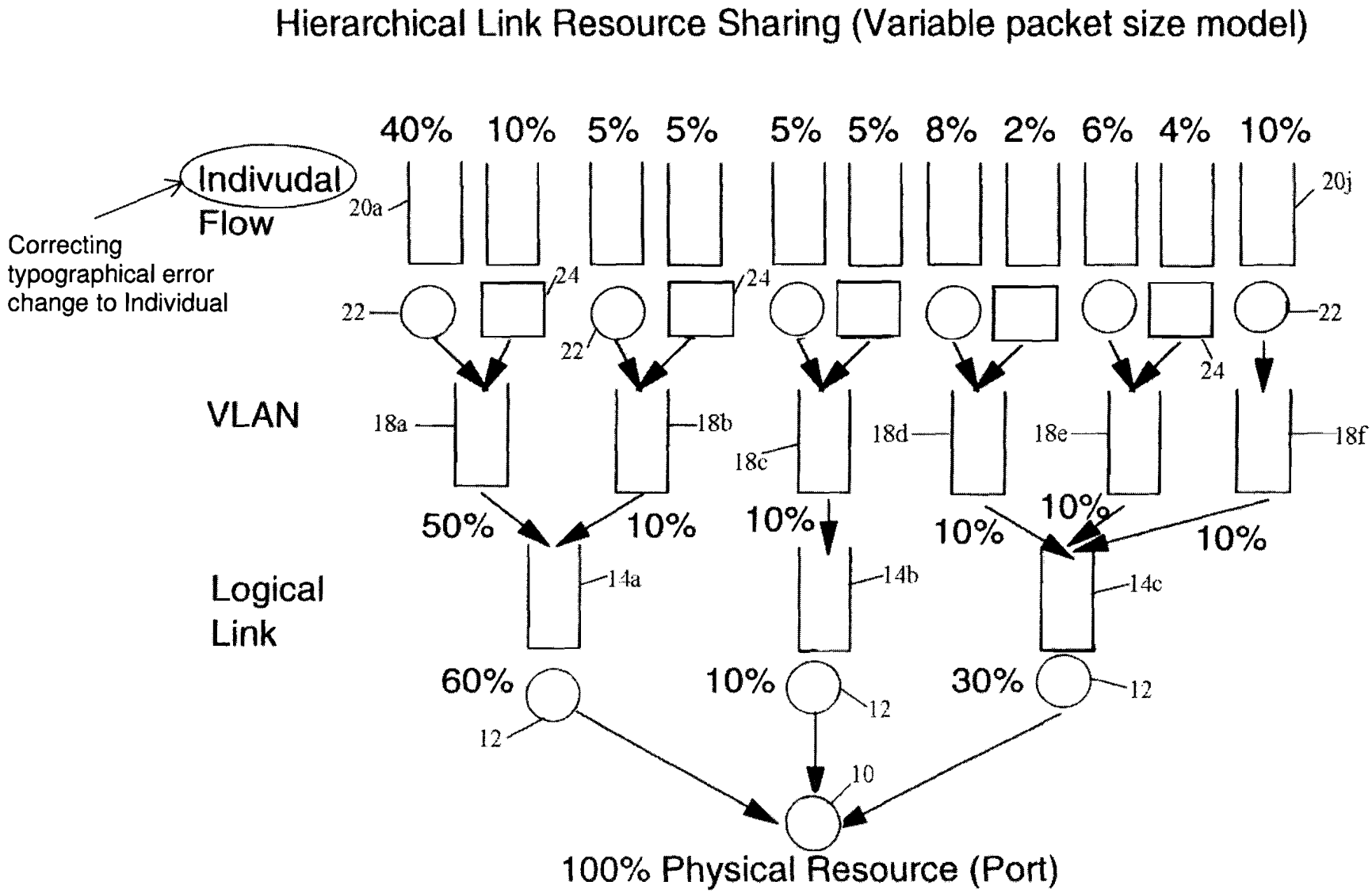
Hierarchical Link Resource Sharing (Variable packet size model)
40%
10%
5%
5%
5%
5%
8%
2%
6%
4%
10%
Indivudal
Flow
Correcting
typographical error
change to Individual
20a
20j
22
24
VLAN
18a
18b
18c
18d
18e
18f
50%
10%
10%
10%
10%
10%
Logical
Link
14a
14b
14c
60%
10%
30%
12
10
100% Physical Resource (Port)

Figure 2